The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for producing an electrical device comprising the steps of:

forming a flat lead frame including a plurality of leads extending radially from a central opening, the lead frame having opposing upper and lower surfaces;

mounting the lead frame and an integrated circuit die onto a strip of adhesive tape such that a lower surface of the die contacts the adhesive tape and the die is located in the central opening, and the lower surface of the lead frame also contacts the adhesive tape;

electrically connecting bond pads on a top surface of the die to associated lead frame leads using wire bonding with the adhesive tape in place such that the adhesive tape holds the die and lead frame in place during the wire bonding operation;

forming a plastic casing over an upper surface of the die and the upper surface of the lead frame wherein the plastic casing comes into contact with the adhesive tape such that a lower surface of the plastic casing is substantially co-planar with the lower surfaces of the lead frame and the die; and

removing the adhesive tape after forming the plastic casing to expose the lower surfaces of the die and the lead frame, whereby exposed surfaces of the lead frame directly form the only externally exposed and accessible I/O contacts for the package and plastic material fills at least portions of gaps between adjacent leads, such that the lower surface of the package is substantially co-planar and includes exposed portions of the plastic casing, the lead frame and the die.

2. (Cancelled)

3. (Cancelled)

4. (Original) The method of claim 1, wherein the step of forming the lead frame comprises etching a metal sheet.

5. (Original) The method of claim 1, wherein the step of forming the lead frame comprises stamping a metal sheet.

6. (Original) The method of claim 1, wherein the step of forming the plastic casing comprises molding plastic onto the upper surfaces of the die and the lead frame.

7. (Currently Amended) A method of packaging an integrated circuit comprising:

providing a lead frame including a plurality of leads and a central opening, the lead frame having opposing upper and lower surfaces;

mounting the lead frame and an integrated circuit die onto a strip of adhesive tape such that a lower surface of the die contacts the adhesive tape and the die is located in the central opening, and the lower surface of the lead frame also contacts the adhesive tape such that the lower surface of the die and the lower surface of the lead frame are substantially co-planar;

electrically connecting bond pads on a top surface of the die to associated lead frame leads using wire bonding with the adhesive tape in place such that the adhesive tape holds the die and lead frame in place during the wire bonding operation;

molding a plastic casing over an upper surface of the die and the upper surface of the lead frame wherein the molded plastic casing comes into contact with the adhesive tape such that a lower surface of the plastic casing is substantially co-planar with the lower surfaces of the lead frame and the die; and

removing the adhesive tape after molding the plastic casing to expose the lower surfaces of the die and the leads, whereby exposed surfaces of the leads directly form the only externally exposed and accessible direct I/O contacts for a resulting integrated circuit package and plastic material fills at least portions of gaps formed between adjacent leads such that the lower surface of the package is substantially co-planar and includes exposed portions of the plastic casing, the lead frame and the die.

8. (Previously Presented) A method as recited in claim 7 further comprising mounting the package on a circuit board such that the lower surface of the die is in direct contact with a heat sink formed on the circuit board.

9. (Previously Presented) A method as recited in claim 7 further comprising applying solder to exposed portions of the leads.

10. (Previously Presented) A method as recited in claim 9 further comprising soldering the lower surfaces of the leads to a circuit board to electrically connect the package to the circuit board.

11. (New) A method as recited in claim 1 further comprising trimming the leads such that peripheral portions of the leads are flush with side surfaces of the plastic casing.

12. (New) A method as recited in claim 7 further comprising trimming the leads such that peripheral portions of the leads are flush with side surfaces of the plastic casing.

13. (New) A method as recited in claim 1 further comprising applying solder to the exposed lower surfaces of the leads.

14. (New) A method as recited in claim 7 further comprising applying solder to the exposed lower surfaces of the leads.

15. (New) A method of packaging an integrated circuit comprising:

providing a lead frame including a plurality of leads and a central opening, the lead frame having opposing upper and lower surfaces;

mounting the lead frame and an integrated circuit die onto a strip of adhesive tape such that a lower surface of the die contacts the adhesive tape and the die is located in the central opening, and the lower surface of the lead frame also contacts the adhesive tape such that the lower surface of the die and the lower surface of the lead frame are substantially co-planar;

electrically connecting bond pads on a top surface of the die to associated lead frame leads using wire bonding with the adhesive tape in place such that the adhesive tape holds the die and lead frame in place during the wire bonding operation;

molding a plastic casing over an upper surface of the die and the upper surface of the lead frame wherein the molded plastic casing comes into contact with the adhesive tape such that a lower surface of the plastic casing is substantially co-planar with the lower surfaces of the lead frame and the die;

cutting at least the lead frame after the molding such that each of the leads is substantially flush with an associated side surface of the casing;

removing the adhesive tape after molding the plastic casing to expose the lower surfaces of the die and the leads, whereby exposed portions of the leads directly form the only externally accessible I/O contacts for a resulting integrated circuit package and plastic material fills at least portions of gaps formed between adjacent leads such that the lower surface of the package is substantially co-planar and includes exposed portions of the plastic casing, the lead frame and the die; and

applying solder to the exposed lower surfaces of the leads.